Impact of Layout Style and Parasitic Capacitances in Full Adder

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I. Introduction

Low power consumption, high speed and small silicon area are the main features of today's growing use of portable electronic devices. Full adders are basic building blocks in microprocessors and digital signal processors.

In this work, two major methodologies to improve the performance of full adder are addressed. One is the architecture approach, by enhancing the features of the full adder at the transistor level design. The other is the technology approach with appropriated layout, by using SOI instead of bulk technology.

Two architectures are presented and compared in this work in order to investigate their performance in terms of power consumption, delay and area namely the conventional Static CMOS full adder and the Hybrid full adder. Further improvements in the above mentioned criterion can be gained by porting the design from bulk to SOI technology.

Using 0.13 μm bulk technology with 1.2 V supply, both full adders are simulated to investigate the effect of the architecture at the gate level. The layouts of the full adders are presented in bulk and SOI technologies to manifest the reduction in area and parasitic capacitance gained by using the SOI technology.

II. Architecture

The Static CMOS full adder [1] shown in Fig. 1 is very popular due to its robustness and scalability at low voltages. However, its transistor count (28), power consumption and critical path delay are being addressed in literature as being no longer suitable for low power arithmetic circuits.

A new Hybrid full adder, shown in Fig. 2, was presented in [2], using the low power XNOR gates proposed in [3] in the sum module. The low power XNOR suffers from a weak "1" logic for (in1, in2) = (1,1) configuration since an NMOS pass gate drives the output node to (V_{DD} - V_{tn}). Therefore, a CMOS inverter is used to enhance the output driving capability. The carry module is identical to that of the Static CMOS full adder without the output inverter. This requires inverted inputs to the next driven full adder with a slight modification in the sum module.

The Hybrid and Static CMOS full adders are simulated in SPICE using the same W/L ratio shown in Fig. 1. Both full adders are driven by two inverters and loaded by a similar type of full adder as shown in Fig. 3. Table I summarizes the gate level simulation results of the adders using bulk technology. The Hybrid full adder shows a reduction of 4.4% in terms of power at 100 MHz, 15.4% in sum delay, 5.8% in carry delay and 19.2% in Power-Delay Product (PDP).

III. Layout Impact on Full Adder

SOI technology allows the layout to be more compact due to the elimination of wells and body contacts as compared to Bulk technology; this allows the designer to freely place NMOS and PMOS transistors nevertheless share their diffusions, which further reduces the area. A significant reduction in junction capacitance is another important aspect of SOI [4]. Figures 4 and 5 show the layouts of the Hybrid full adder in Bulk and SOI technologies, respectively. SOI layout reduces the area of the Hybrid full adder by 13.5% and that of the Static CMOS by 17.4% as shown in Table II. The effect of parasitic capacitance reduction in SOI is addressed as SOI-1 while the effect of reducing both the parasitic and the diffusion capacitance in SOI is addressed as SOI-2. Fig. 6 shows the gate, diffusion capacitance, routing capacitance and total powers of the Hybrid full adder implemented in Bulk, SOI-1 and SOI-2 at 100 MHz. The absolute power values are shown in μW inside the bars. It can be seen that the gate power is 60% of the total power in Bulk while it is 64.2% in SOI-1 and 70.4% in SOI-2 which indicates the trend of having the gate power closer to 100% in the ideal case. Table III shows a reduction in the total power of the Static CMOS full adder of 10.5% when SOI-1 is used and a reduction of 16% when SOI-2 is used. The sum delay reduction is 6.3% when SOI-1 is used and 12.6% when SOI-2 is used. Also the PDP is reduced by 16.1% when using SOI-1 and by 26.6% using SOI-2. Almost the same conclusions can be drawn from Table IV showing the results of the Hybrid full adder.

IV. Conclusions

This work presents the impact of varying both the architecture and the technology on the performance of the full adder. A 10% reduction in total power and 15.2% reduction in delay are gained by changing the architecture. While an average power reduction of 15.5% and 14.1% reduction in average delay are gained by using SOI layout and junction capacitances instead of Bulk.

References

[1] K. Martin, Oxford University Press, 2000.
[2] I. Hassoune, PhD Thesis, UCL, Belgium, 2006.
[3] J.-M. Wang *et al.*, *IEEE Journal of Solid-State Circuits*, Jul. 1994.
[4] J.-P. Colinge, 3rd Edition, Kluwer Academic Publishers, 2004.

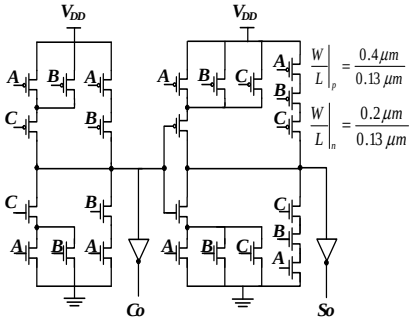

Fig. 1. Schematic of Static CMOS full adder.

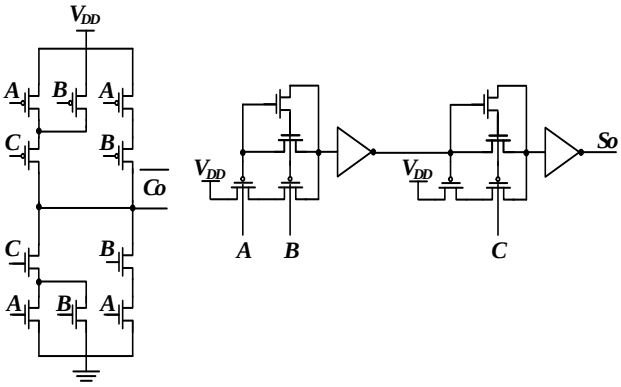

Fig. 2. Schematic of Hybrid full adder.

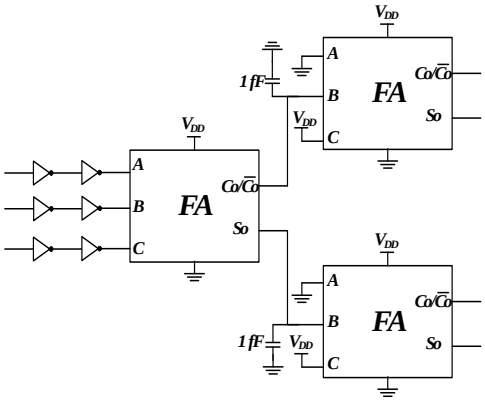

Fig. 3. Simulation Test bench.

TABLE I

SIMULATION RESULTS FOR HYBRID AND STATIC CMOS FULL ADDER.

	Power (μW)	Sum Delay (ps)	Carry Delay (ps)	PDP (sum) (*E-18)
Static CMOS	1.13	175	120	198
Hybrid	1.08	148	113	160

TABLE II

AREA COMPARISON.

	Bulk	SOI
Static CMOS	28.6 μm^2	23.62 μm^2
Hybrid	23.02 μm^2	19.9 μm^2

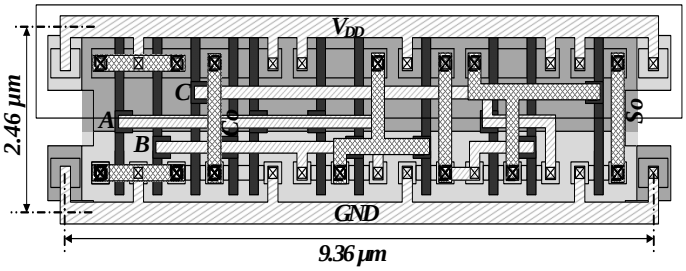

Fig. 4. Bulk layout of Hybrid full adder.

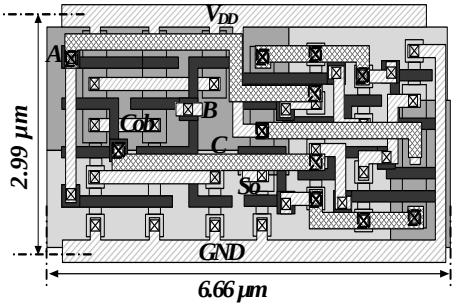

Fig. 5. SOI layout of Hybrid full adder.

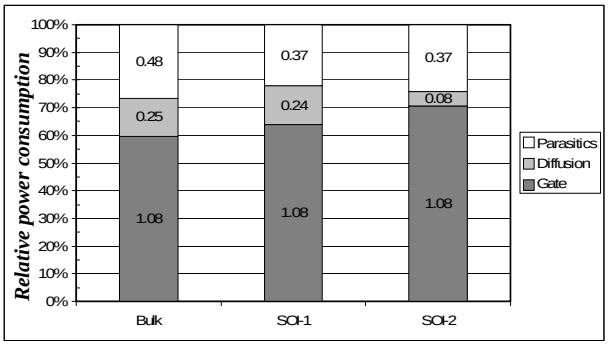

Fig. 6. Effect of diffusion and parasitic on Hybrid full adder Power. Absolute values are shown inside the bars in μW.

TABLE III

STATIC CMOS FULL ADDER POST-LAYOUT SIMULATION RESULTS.

	Bulk	SOI–1	SOI–2
Worst power @ 100 MHz (μW)	2	1.79	1.68
Worst Sum delay (ps)	316	296	276
Worst Carry Delay (ps)	229	209	194
PDP (Sum) (*E-18)	632	530	464

TABLE IV

HYBRID FULL ADDER POST-LAYOUT SIMULATION RESULTS.

	Bulk	SOI–1	SOI–2
Worst power @ 100 MHz (μW)	1.8	1.68	1.53
Worst Sum delay (ps)	268	251	226
Worst Carry Delay (ps)	189	178	162
PDP (Sum) (*E-18)	482	422	346